Claims:

1. A voltage clamping circuit comprising:

an input terminal to which an input voltage is supplied;

a MOSFET which has either one of source/drain routes thereof connected to the input terminal and has a predetermined voltage to be restricted supplied to a gate thereof; and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit, and

the voltage clamping circuit obtains an output voltage from another source/drain route of the MOSFET.

2. A voltage clamping circuit according to claim 1, wherein a capacitor is provided in parallel to the current source.

3. A voltage clamping circuit according to claim 2, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is a depression type MOSFET which connects a gate and a source thereof to each other.

4. A voltage clamping circuit according to claim 3, wherein

the output voltage is supplied to an input of a first CMOS inverter circuit which is operated with a power source voltage smaller than the input voltage, and

the predetermined voltage is the power source voltage.

5. A voltage clamping circuit according to claim 1, wherein

the voltage clamping circuit is mounted on a semiconductor integrated circuit device, and

the input terminal includes an external terminal of the semiconductor integrated circuit device, and an electrostatic breakdown preventing circuit is provided thereto.

6. A voltage clamping circuit according to claim 5, wherein

an output signal of the first CMOS inverter circuit is transmitted to an input of a second CMOS inverter circuit on a next stage, and

an output signal of the second CMOS inverter circuit is fed back to a gate of the MOSFET which is provided between an input terminal of the circuit and a ground potential of the circuit thus allowing a first CMOS inverter circuit to possess a hysteresis transmission characteristic.

7. A voltage clamping circuit according to claim 5, wherein

the MOSFET and the depression MOSFET are of an N-channel type, and

the input voltage and the power source voltage assume positive voltages.

8. A voltage clamping circuit according to claim 1, wherein

the current source allows a DC current component to flow therethrough.

9. A voltage clamping circuit according to claim 8, wherein

a capacitor is provided in parallel to the current source.

10. A voltage clamping circuit according to claim 9,

wherein

the output voltage is supplied to an input part of an input circuit which is operated with a power source voltage smaller than the input voltage, and the predetermined voltage is the power source voltage, and

the input circuit includes a capacitive component in parallel to the capacitor.

11. A voltage clamping circuit according to claim 1, wherein

a substrate of the MOSFET is connected to another source/drain route of the MOSFET.

12. A voltage level shifting circuit comprising:

a MOSFET which has either one of source/drain routes thereof connected to an input node to which an input voltage is supplied and has a predetermined voltage to be restricted supplied to a gate thereof;

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit and allows a DC current component to flow therethrough; and

the voltage level shifting circuit obtains an output voltage from another source/drain route of the MOSFET.

13. A voltage level shifting circuit according to claim 12, wherein

a capacitor is provided in parallel to the current source.

14. A voltage level shifting circuit according to claim 13, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is a depression type MOSFET which connects a gate and a source thereof to each other.

15. A voltage level shifting circuit according to claim 14, wherein

the output voltage is supplied to an input of a first CMOS inverter circuit which is operated with a power source voltage smaller than the input voltage, and

the predetermined voltage is the power source voltage.

16. A voltage level shifting circuit according to claim 12, wherein

the voltage level shifting circuit is mounted on one semiconductor substrate.

17. A voltage level shifting circuit according to claim 16, wherein

the voltage level shifting circuit is mounted on a semiconductor integrated circuit device, and

the input node is an external terminal of the semiconductor integrated circuit device, and an electrostatic breakdown preventing circuit is provided thereto.

18. A voltage level shifting circuit according to claim

17, wherein

an output signal of the first CMOS inverter circuit is transmitted to an input of a second CMOS inverter circuit on a next stage, and

an output signal of the second CMOS inverter circuit is fed back to a gate of the MOSFET which is provided between an input terminal of the circuit and a ground potential of the circuit thus allowing a first CMOS inverter circuit to possess a hysteresis transmission characteristic.

19. A voltage level shifting circuit according to claim 14, wherein

the MOSFET and the depression MOSFET are of an N-channel type, and

the input voltage and the power source voltage assume positive voltages.

20. A voltage level shifting circuit according to claim 13, wherein

the output voltage is supplied to an input part of an input circuit which is operated with a power source voltage smaller than the input voltage,

the predetermined voltage is the power source voltage, and

the input circuit includes a capacitive component in parallel to the capacitor.

21. A voltage level shifting circuit according to claim

12, wherein

a substrate of the MOSFET is connected to another source/drain route of the MOSFET.

22. A switching power source device comprising;

an inductor;

a capacitor which is provided in series with the inductor and forms an output voltage;

a first switching element which controls a current which is made to flow in the inductor based on an input voltage;

a second switching element which clamps another terminal other than a terminal which forms the output voltage of the inductor at a first predetermined voltage when the first switching element assumes an OFF state;

a first driving circuit which drives the first switching element using a first voltage signal corresponding to the input voltage;

a second driving circuit which drives the second switching element using a second voltage;

a control circuit which is operated by the input voltage or a third voltage which is equal to or less than the second voltage, and forms a PWM signal so that the output voltage which is obtained from the capacitor becomes a second predetermined voltage;

a control logic circuit which is operated by the third voltage, and forms a driving signal for the first driving circuit

and the second driving circuit by receiving the PWM signal, wherein

the control logic circuit includes a first voltage clamping circuit which performs voltage clamping of a driving signal of the first switching element in response to the third voltage and feedbacks the driving signal of the first switching element to an input of the second driving circuit, and a second voltage clamping circuit which performs voltage clamping of a driving signal of the second switching element in response to the low voltage and feedbacks the driving signal of the second switching element to an input of the first driving circuit, and performs a switching control to prevent the first and second switching elements from simultaneously assuming an ON state, and

the voltage clamping circuit includes

an input node to which the driving signal is supplied,

a MOSFET which has either one of source/drain routes connected to the input node and the third voltage supplied to a gate thereof; and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit, and

the voltage clamping circuit obtains a feedback signal which is generated by performing the voltage clamping of the driving signal from another source/drain route of the MOSFET.

23. A switching power source device according to claim

22, wherein

the switching power source device includes a third clamping circuit, and

the third clamping circuit is constituted of

an input node to which an input signal for controlling an active/reactive (ON/OFF) state of the switching power source device is supplied,

a MOSFET which has either one of the source/drain routes thereof connected to the input node and has the third voltage supplied to a gate thereof, and

a current source which is provided between another source/drain route of the MOSFET and the ground potential of the circuit, wherein

the third voltage clamping circuit obtains a control signal which is generated by performing the voltage clamping of the input signal from another source/drain route of the MOSFET.

24. A switching power source device according to claim 23, wherein

a capacitor is provided in parallel to the current source.

25. A switching power source device according to claim 24, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is formed of a depression type MOSFET

which connects a gate and a source thereof to each other.

26. A switching power source device according to claim 23, wherein

the current source allows a DC current component to flow therethrough.

27. A switching power source device according to claim 26, wherein

a capacitor is provided in parallel to the current source.

28. A switching power source device according to claim 27, wherein

the feedback signal is supplied to an input part of the control logic circuit which is operated with a power source voltage smaller than the driving signal.

29. A semiconductor integrated circuit device comprising;

a first switching element which controls a current for forming an output voltage by dropping an input voltage;

a terminal which allows the current to pass therethrough;

a second switching element which clamps the terminal at a predetermined potential when the first switching element assumes an OFF state;

a first driving circuit which drives the first switching element using a first voltage signal corresponding to the input voltage;

a second driving circuit which drives the second switching element using a second voltage; and

a control logic circuit which is operated by the input voltage or a third voltage which is equal to or less than the second voltage, and forms a driving signal for the first driving circuit and the second driving circuit by receiving a PWM signal, wherein

the control logic circuit includes a first voltage level shifting circuit which shifts a voltage level of a driving signal of the first switching element in response to the third voltage and feedbacks the driving signal of the first switching element to an input of the second driving circuit, and a second voltage level shifting circuit which shifts a voltage level of a driving signal of the second switching element in response to the low voltage and feedbacks the driving signal of the second switching element to an input of the first driving circuit, and performs a switching control to prevent the first and second switching elements from simultaneously assuming an ON state,

the first switching element is formed on a first semiconductor substrate,

the second switching element is formed on a second semiconductor substrate,

the first driving circuit, the second driving circuit, the control logic circuit, and the first and second voltage level shifting circuits are formed on a third semiconductor substrate, and

the first, second and third semiconductor substrates are

sealed in one package.

30. A semiconductor integrated circuit device according to claim 29, wherein

the first and second voltage level shifting circuits include

an input node to which the driving signal is supplied,

a MOSFET which has either one of source/drain routes thereof connected to the input node and has the third voltage supplied to the gate thereof, and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit and allows a DC current component to flow therethrough, wherein

the semiconductor integrated circuit device obtains a feedback signal which is generated by shifting a voltage level of the driving signal from another source/drain route of the MOSFET.

31. A semiconductor integrated circuit device according to claim 29, wherein

the circuit device includes a third voltage level shifting circuit,

the third voltage level shifting circuit is formed on the third semiconductor substrate,

the third voltage level shifting circuit obtains

an input terminal to which an input signal for controlling

an active/reactive (ON/OFF) state of the switching power source device is supplied,

a MOSFET which has either one of the source/drain routes thereof connected to the input terminal and has the third voltage supplied to the gate thereof, and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of a circuit and allows a DC current component to flow therethrough, and

the third voltage level shifting circuit obtains a control signal which is formed by shifting a voltage level of the input signal from another source/drain route of the MOSFET.

32. An IC according to claim 30, wherein

a capacitor is provided in parallel to the power source.

33. A semiconductor integrated circuit device according to claim 32, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is a depression type MOSFET which connects a gate and a source thereof to each other.

34. A semiconductor integrated circuit device according to claim 30, wherein

the feedback signal is transmitted to an input part of the control logic circuit which is operated with a power source

voltage smaller than the driving signal.

35. A semiconductor integrated circuit device according to claim 29, wherein

the current is a current which is made to flow in the inductor from the input voltage to form the output voltage by the inductor and the capacitor which is provided in series with the inductor.

36. A semiconductor integrated circuit device according to claim 35 wherein

a counter-electromotive voltage which is generated in the inductor is clamped by clamping the terminal at the predetermined potential.

37. A voltage level shifting circuit comprising;

an input terminal to which an input voltage is supplied;

a MOSFET which has either one of source/drain routes thereof connected to the input terminal and has a predetermined voltage to be restricted supplied to a gate thereof, wherein

a substrate of the MOSFET is connected to another source/drain route of the MOSFET, and an output voltage is obtained from another source/drain route of the MOSFET.

38. A voltage level shifting circuit according to claim 37, wherein the voltage level shifting circuit includes a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit.

39. A voltage level shifting circuit according to claim 38, wherein

a capacitor is provided in parallel to the current source.

40. A voltage level shifting circuit according to claim 39, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is a depression type MOSFET which connects a gate and a source thereof to each other.

41. A voltage level shifting circuit according to claim 37, wherein

the output voltage is supplied to an input of a first CMOS inverter circuit which is operated with a power source voltage smaller than the input voltage, and

the predetermined voltage is the power source voltage.

42. A voltage level shifting circuit according to claim 37, wherein

the voltage clamping circuit is mounted on a semiconductor integrated circuit device, and

the input terminal is an external terminal of the semiconductor integrated circuit device and an electrostatic breakdown preventing circuit is provided thereto.

43. A voltage level shifting circuit according to claim 41, wherein

an output signal of the first CMOS inverter circuit is transmitted to an input of a second CMOS inverter circuit on

a next stage, and

an output signal of the second CMOS inverter circuit is fed back to a gate of a MOSFET which is provided between an input terminal of the second CMOS inverter circuit and a ground potential of the circuit thus allowing the first CMOS inverter circuit to possess a hysteresis transmission characteristic.

44. A voltage level shifting circuit according to claim 40, wherein

the MOSFET and the depression MOSFET are of an N-channel type, and

the input voltage and the power source voltage assume positive voltages.

45. A voltage level shifting circuit according to claim 38, wherein

the current source allows a DC current component to flow therethrough.

46. A voltage level shifting circuit according to claim 45, wherein

a capacitor is provided in parallel to the current source.

47. A voltage level shifting circuit according to claim 46, wherein

the output voltage is supplied to an input part of an input circuit which is operated with a power source voltage smaller than the input voltage, and the predetermined voltage is the power source voltage, and

the input circuit includes a capacitive component in parallel to the capacitor.